



DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller

Data Sheet

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Digital Equipment Corporation
Maynard, Massachusetts

<http://www.digital.com/semiconductor>

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1 DIGITAL Semiconductor 21143 Overview

The DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (21143) supports the peripheral component interconnect (PCI) bus or CardBus. It provides a direct interface connection to the PCI bus and adapts easily to the CardBus and most other standard buses. The 21143 software interface and data structures are optimized to minimize the host CPU load and to allow for maximum flexibility in the buffer descriptor management. The 21143 contains large onchip FIFOs, so no additional onboard memory is required. The 21143 also provides an upgradable boot ROM interface.

1.1 General Description

The 21143 is an Ethernet LAN controller for both 100-Mb/s and 10-Mb/s data rates, which provides a direct interface to the peripheral component interconnect (PCI) local bus or the CardBus. The 21143 interfaces to the host processor by using onchip command and status registers (CSRs) and a shared host memory area, set up mainly during initialization. This minimizes processor involvement in the 21143 operation during normal reception and transmission.

The 21143 is optimized for low power PCI/CardBus based systems and supports two types of power-management mechanisms. The main mechanism is based upon the OnNow architecture, which is required for PC 97 and PC 98.¹ The alternative mechanism is based upon the older remote wake-up-LAN mechanism.

Large FIFOs allow the 21143 to efficiently operate in systems with longer latency periods. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without a repeated fetch from the host memory. The 21143 provides an upgradable boot ROM interface.

The 21143 provides three network ports: a 10BASE-T 10-Mb/s port, an attachment unit interface (AUI) 10-Mb/s port, and a media-independent/symbol interface (MII/SYM) 10/100-Mb/s port. The 10BASE-T port provides a direct Ethernet connection to the twisted-pair (TP) interface. The AUI port provides a direct Ethernet connection to the AUI.

¹This feature is only supported in the 21143-PD and the 21143-TD.

Features

The MII/SYM port supports two operational modes:

- MII mode—A full implementation of the MII standard
- SYM mode—Symbol interface to an external 100-Mb/s front-end decoder (ENDEC). In this mode the 21143 uses an onchip physical coding sublayer (PCS) and a scrambler/descrambler circuit to enable a low-cost 100BASE-T implementation.

The 21143 is capable of functioning in a full-duplex environment for the MII/SYM and 10BASE-T ports.

1.2 Features

The 21143 has the following features:

Power Management and Power Savings:

- Fully compliant with Revision 1.0 of the *Network Device Class Power Management Specification*, under the OnNow Architecture for Microsoft's *PC 97 Hardware Design Guide* and *PC 98 System Design Guide*.¹
- Supports all wake-up events defined in Revision 1.0 of the *Network Device Class Power Management Specification*, including:¹
 - Pattern matching
 - Link change
 - Magic Packet
- Fully compliant with Revision 1.0 of the *Advanced Configuration and Power Interface (ACPI) Specification*.¹
- Fully compliant with Revision 1.0 of the *PCI Bus Power Management Interface Specification*.¹
- Implements low-power management with two power-saving modes (sleep and snooze), with the device powering up in sleep mode. Powering up in sleep mode allows CardBus PC cards to meet the requirement of consuming less than 70 mA of supply current after power-up.
- Supports remote wake-up-LAN, which is a feature based upon Advanced Micro Device's Magic Packet technology that allows sleeping workstations to be remotely powered up.

¹This feature is only supported in the 21143-PD and the 21143-TD.

- Supports SecureON, which is a security feature that can be added to the Advanced Micro Device's Magic Packet technology.
- Implements low-power, 3.3-V CMOS technology.

PCI and CardBus Features:

- Supports PCI and CardBus interfaces.
- Supports PCI/CardBus clock control through clkrun.
- Supports CardBus **cstschg** pin and Status Changed registers.
- Supports automatic loading of subvendor ID and CardBus card information structure (CIS) pointer from serial ROM to configuration registers.
- Supports storage of CardBus card information structure (CIS) in the serial ROM or the expansion ROM.¹
- Supports the advanced PCI/CardBus read multiple, read line, and write and invalidate commands.
- Supports an unlimited PCI/CardBus burst.
- Supports PCI/CardBus clock speed frequency from dc to 33 MHz; network operation with PCI clock from 20 MHz to 33 MHz.

Host Interface Features:

- Includes a powerful onchip direct memory access (DMA) with programmable burst size, providing low CPU utilization.
- Supports early interrupt on transmit and receive.
- Supports interrupt mitigation on transmit and receive.²
- Supports big or little endian byte ordering for buffers and descriptors.
- Implements unique, patent-pending intelligent arbitration between DMA channels to minimize underflow and overflow.
- Contains large independent receive and transmit FIFOs.

¹For the 21143–PB, 21143–TB, 21143–PC, and the 21143–TC, the CIS can only be stored in the expansion ROM.

²This feature is only supported in the 21143–PD and the 21143–TD.

Features

Network Side Features:

- Supports three network ports: 10BASE-T (10 Mb/s), AUI (10 Mb/s), and MII/SYM (10/100 Mb/s).
- Contains a variety of flexible address filtering modes.
- Contains onchip PCS and scrambler/descrambler for 100BASE-TX.
- Implements signal-detect filtering to avoid false detection of link with 100BASE-TX symbol interfaces.¹
- Enables automatic detection and correction of 10BASE-T receive polarity.
- Contains onchip integrated AUI port and a 10BASE-T transceiver.
- Supports autodetection between 10BASE-T, AUI, and MII/SYM ports.
- Supports IEEE 802.3 Auto-Negotiation algorithm of full-duplex and half-duplex operation for 10 Mb/s and 100 Mb/s (NWAY).
- Offers a unique, patented solution to Ethernet capture-effect problem.
- Supports full-duplex operation on both MII/SYM and 10BASE-T ports.
- Provides internal and external loopback capability on all network ports.
- Supports IEEE 802.3 and ANSI 8802-3 Ethernet standards.

Other Features:

- Provides MicroWire interface for serial ROM (1K and 4K EEPROM).
- Provides an upgradable boot ROM interface up to 256KB.
- Provides LED indications for various network activity.
- Supports interrupts from two general-purpose pins.
- Implements test-access port (JTAG-compatible) with boundary-scan pins.
- Contains a 4-bit, general-purpose programmable register and corresponding I/O pins with the ability to generate interrupts from two general-purpose pins.

¹This feature is only supported in the 21143-PD and the 21143-TD.

1.3 Microarchitecture

The following list describes the 21143 hardware components, and Figure 1 shows a block diagram of the 21143:

- PCI/CardBus interface—Includes all interface functions to the PCI and CardBus bus; handles all interconnect control signals; and executes DMA and I/O transactions
- Boot ROM port—Provides an interface to perform read and write operations to the boot ROM; supports accesses to bytes or longwords (32-bit); and provides the ability to connect an external 8-bit register to the boot ROM port
- Serial ROM port—Provides a direct interface to a MicroWire ROM for storage of the Ethernet address and system parameters
- General-purpose register—Enables software use for input or output functions and LEDs
- DMA—Contains independent receive and transmit controllers; handles data transfers between CPU memory and onchip memory
- FIFOs—Contains independent FIFOs for receive and transmit; supports automatic packet deletion on receive (runt packets or after a collision) and packet retransmission after a collision on transmit
- RxM—Handles all CSMA/CD¹ receive operations, and transfers the network data from the ENDEC to the receive FIFO
- TxM—Handles all CSMA/CD MAC² transmit operations, and transfers data from transmit FIFO to the ENDEC for transmission
- SIA interface—Performs 10-Mb/s physical layer network operations; implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions
- NWAY—Implements the IEEE 802.3 Auto-Negotiation algorithm
- Physical coding sublayer—Implements the encoding and decoding sublayer of the 100BASE-TX (CAT5) specification, including the squelch feature
- Scrambler/descrambler—Implements the twisted-pair physical layer medium dependent (TP-PMD) scrambler/descrambler scheme for 100BASE-TX

¹Carrier-sense multiple access with collision detection.

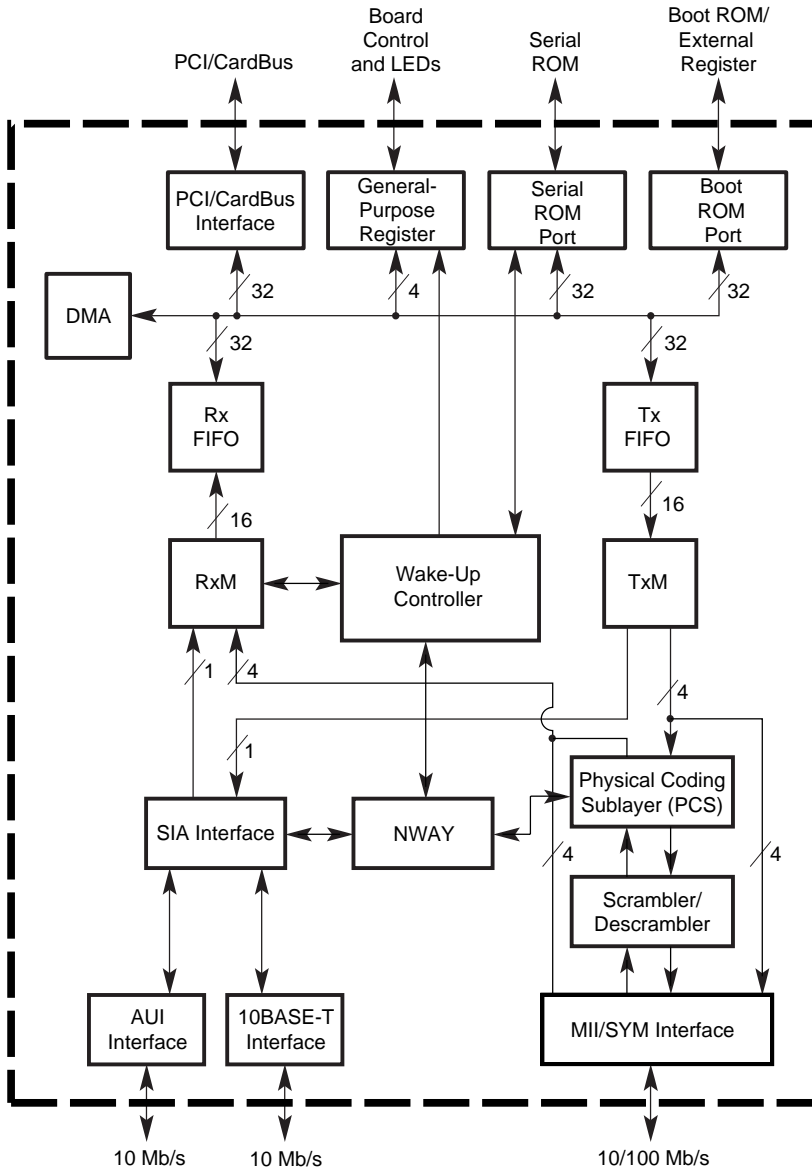
²Media access control.

Microarchitecture

- Three network interfaces—An AUI interface, a 10BASE-T interface, and an MII/SYM interface provide a full MII signal interface and direct interface to the 100-Mb/s ENDEC for CAT5
- Wake-up-controller—Enables power-management control compliant with the ACPI¹ and remote power-up capabilities using the remote wake-up-LAN mechanism

¹This feature is only supported in the 21143-PD and the 21143-TD.

Figure 1 21143 Block Diagram



FM-06117.A14

2 Pinout

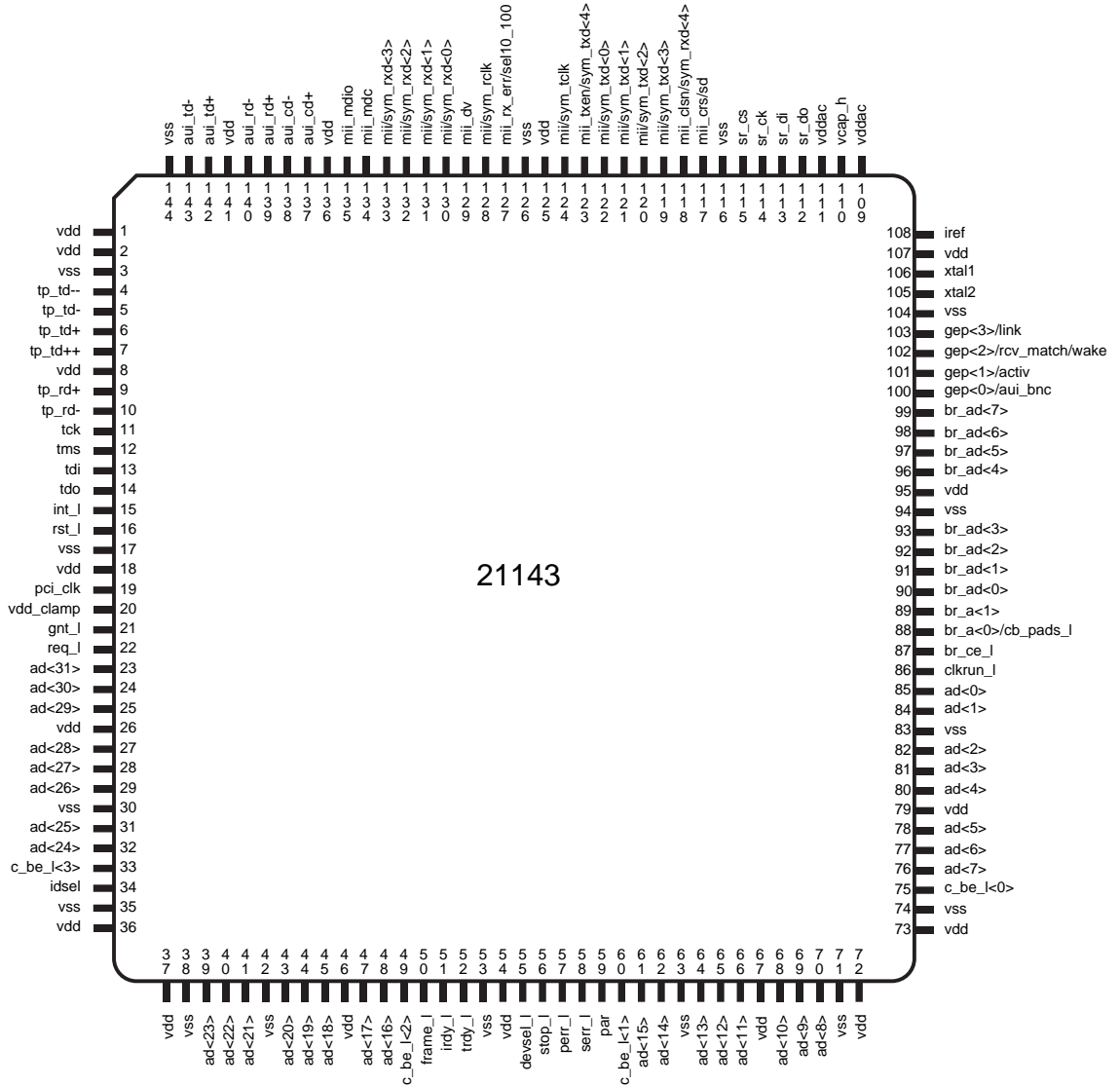
The 21143 is offered in two package styles: a 144-pin low-profile quad flat pack (LQFP) and a 144-pin metric quad flat pack (MQFP). The tables in this section provide a description of the pins and their respective signal definitions.

Table 1 lists the tables in this section. Figure 2 shows the 21143 pinout for both the LQFP and MQFP package types.

Table 1 Index to Pinout Tables

For this information...	Refer to...
Logic signals	Table 2
Power pins	Table 3
Functional signals description	Table 4
Input pins	Table 5
Output pins	Table 6
Input/output pins	Table 7
Open drain pins	Table 8
Signal functions	Table 9

Figure 2 21143 Pinout Diagram (Top View)



LJ-04940.A14

Signal Reference Tables

2.1 Signal Reference Tables

Table 2 provides an alphabetical list of the 21143 logic names and their pin numbers.
Table 3 provides a list of the 21143 power pin numbers.

Table 2 Logic Signals

(Sheet 1 of 2)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
ad<0>	85	ad<24>	32	br_ce_1	87
ad<1>	84	ad<25>	31	c_be_1<0>	75
ad<2>	82	ad<26>	29	c_be_1<1>	60
ad<3>	81	ad<27>	28	c_be_1<2>	49
ad<4>	80	ad<28>	27	c_be_1<3>	33
ad<5>	78	ad<29>	25	clkrun_1	86
ad<6>	77	ad<30>	24	devsel_1	55
ad<7>	76	ad<31>	23	frame_1	50
ad<8>	70	au_i_cd-	138	gep<0>/au_i_bnc	100
ad<9>	69	au_i_cd+	137	gep<1>/activ	101
ad<10>	68	au_i_rd-	140	gep<2>/rcv_match/wake	102
ad<11>	66	au_i_rd+	139	gep<3>/link	103
ad<12>	65	au_i_td-	143	gnt_1	21
ad<13>	64	au_i_td+	142	idsel	34
ad<14>	62	br_a<0>/cb_pads_1	88	int_1	15
ad<15>	61	br_a<1>	89	irdy_1	51
ad<16>	48	br_ad<0>	90	iref	108
ad<17>	47	br_ad<1>	91	mii_clsn/sym_rxd<4>	118
ad<18>	45	br_ad<2>	92	mii_crs/sd	117
ad<19>	44	br_ad<3>	93	mii_dv	129
ad<20>	43	br_ad<4>	96	mii_mdc	134
ad<21>	41	br_ad<5>	97	mii_mdio	135
ad<22>	40	br_ad<6>	98	mii/sym_rclk	128
ad<23>	39	br_ad<7>	99	mii_rx_err/sel10_100	127

Signal Reference Tables

Table 2 Logic Signals

(Sheet 2 of 2)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
mii/sym_rxd<0>	130	perr_l	57	tms	12
mii/sym_rxd<1>	131	req_l	22	tp_rd-	10
mii/sym_rxd<2>	132	rst_l	16	tp_rd+	9
mii/sym_rxd<3>	133	serr_l	58	tp_td-	5
mii/sym_tclk	124	sr_ck	114	tp_td- -	4
mii/sym_txd<0>	122	sr_cs	115	tp_td+	6
mii/sym_txd<1>	121	sr_di	113	tp_td+ +	7
mii/sym_txd<2>	120	sr_do	112	trdy_l	52
mii/sym_txd<3>	119	stop_l	56	vcap_h	110
mii_txen/sym_txd<4>	123	tck	11	xtal1	106
par	59	tdi	13	xtal2	105
pci_clk	19	tdo	14	—	—

Table 3 Power Pins

Signal	Pin Number	Signal	Pin Number
vdd (3.3 V)	1, 2, 8, 18, 26, 36, 37, 46, 54, 67, 72, 73, 79, 95, 107, 125, 136, 141	vss (GND)	3, 17, 30, 35, 38, 42, 53, 63, 71, 74, 83, 94, 104, 116, 126, 144
vddac (3.3 V)	109, 111	—	—
vdd_clamp (5 V or 3.3 V)	20	—	—

Signal Reference Tables

The functional grouping of each pin is listed in Section 2.3.

The following terms describe the 21143 pinout:

- **Address phase**

Address and appropriate bus commands are driven during this cycle.

- **Data phase**

Data and the appropriate byte enable codes are driven during this cycle.

- **_l**

All pin names with the **_l** suffix are asserted low.

The following pins in Table 4 have an internal pull-up:

tms

tdi

br_ce_l

sr_do

mii/sym_tclk

Pin **sr_cs** has an internal pull-down.

Table 4 uses the following abbreviations:

I = Input

O = Output

I/O = Input/output

O/D = Open drain

P = Power

Signal Reference Tables

Table 4 provides a functional description of each of the 21143 signals. These signals are listed alphabetically

Table 4 Functional Description of 21143 Signals

(Sheet 1 of 11)

Signal	Type	Pin Number	Description
ad<31:0>	I/O	23, 24, 25, 27, 28, 29, 31, 32, 39, 40, 41, 43, 44, 45, 47, 48, 61, 62, 64, 65, 66, 68, 69, 70, 76, 77, 78, 80, 81, 82, 84, 85	32-bit PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, the address bits contain a physical address (32 bits). During subsequent clock cycles, these same lines contain 32 bits of data. A 21143 bus transaction consists of an address phase followed by one or more data phases. The 21143 supports both read and write bursts (in master operation only). Little and big endian byte ordering can be used.
au_i_cd-	I	138	Attachment unit interface receive collision differential negative data.
au_i_cd+	I	137	Attachment unit interface receive collision differential positive data.
au_i_rd-	I	140	Attachment unit interface receive differential negative data.
au_i_rd+	I	139	Attachment unit interface receive differential positive data.
au_i_td-	O	143	Attachment unit interface transmit differential negative data.
au_i_td+	O	142	Attachment unit interface transmit differential positive data.

Signal Reference Tables

Table 4 Functional Description of 21143 Signals

(Sheet 2 of 11)

Signal	Type	Pin Number	Description
br_a<0>/cb_pads_l	O	88	<p>Boot ROM address line bit 0. In a 256KB configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17.</p> <p>This pin also determines the type of signals to use for the PCI/CardBus output pins, either PCI or CardBus.¹ By default, this pin selects PCI signaling. To select CardBus signaling, this pin must be connected to a pull-down resistor.</p> <p>Note: The 21143–PB, 21143–TB, 21143–PC, and the 21143–TC only support signaling for PCI. To meet the signaling requirements for CardBus, external series resistors must be added to these devices.</p>
br_a<1>	O	89	<p>Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches.</p>
br_ad<7:0>	I/O	90, 91, 92, 93, 96, 97, 98, 99	<p>Boot ROM address and data multiplexed lines bits 7 through 0. In two consecutive address cycles, these lines contain the boot ROM address pins 7 through 2, oe_l and we_l in the first cycle; and these lines contain boot ROM address pins 15 through 8 in the second cycle. During the data cycle, bits 7 through 0 contain data.</p>
br_ce_l	O	87	<p>Boot ROM or external register chip enable.</p>
c_be_l<3:0>	I/O	33, 49, 60, 75	<p>Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins.</p> <p>During the address phase of the transaction, these 4 bits provide the bus command.</p> <p>During the data phase, these 4 bits provide the byte enable. The byte enable determines which byte lines carry valid data. For example, bit 0 applies to byte 0, and bit 3 applies to byte 3.</p>

Table 4 Functional Description of 21143 Signals

(Sheet 3 of 11)

Signal	Type	Pin Number	Description
clkrun_1	I/O O/D	86	<p>PCI/CardBus clock run indication. The host system asserts this signal to indicate normal operation of the clock. The host system deasserts clkrun_1 when the clock is going to be stopped or slowed down to a nonoperational frequency.</p> <p>If the clock is needed by the 21143, the 21143 asserts clkrun_1, requesting normal clock operation to be maintained or restored. Otherwise, the 21143 allows the system to stop the clock.</p> <p>Note: The 21143–PB, 21143–TB, 21143–PC, and the 21143–TC continuously request the host for the clock, which prevents the clock from stopping or slowing down.</p>
devsel_1	I/O	55	<p>Device select is asserted by the target of the current bus access. When the 21143 is the initiator of the current bus access, it expects the target to assert devsel_1 within 5 bus cycles, confirming the access. If the target does not assert devsel_1 within the required bus cycles, the 21143 aborts the cycle. To meet the timing requirements, the 21143 asserts this signal in a medium speed (within 2 bus cycles).</p>
frame_1	I/O	50	<p>The frame_1 signal is driven by the bus master to indicate the beginning and duration of an access. The frame_1 signal asserts to indicate the beginning of a bus transaction. While frame_1 is asserted, data transfers continue. The frame_1 signal deasserts to indicate that the next data phase is the final data phase transaction.</p>

Signal Reference Tables

Table 4 Functional Description of 21143 Signals

(Sheet 4 of 11)

Signal	Type	Pin Number	Description
gep<0>/aui_bnc	I/O	100	<p>This pin can be configured by software to be:</p> <ul style="list-style-type: none"> • A general-purpose pin that performs either input or output functions. This general-purpose pin can provide an interrupt when functioning as an input. • A control pin that provides an AUI (10BASE5) or BNC (10BASE2) select line. <p>This control pin is mainly used to enable the external BNC transceiver in 10BASE2 mode. When set, the 10BASE5 mode is selected. When reset, the 10BASE2 mode is selected.</p> <p>Note: This control pin is internally forced to the aui_bnc function when the 21143 is in remote wake-up-LAN mode.</p>
gep<1>/activ	I/O	101	<p>This pin can be configured by software to be:</p> <ul style="list-style-type: none"> • A general-purpose pin that performs either input or output functions. This general-purpose pin can provide an interrupt when functioning as an input. • A status pin that provides an LED that indicates either receive or transmit activity.
gep<2>/rcv_match/wake	I/O	102	<p>This pin can be configured by software to be:</p> <ul style="list-style-type: none"> • A general-purpose pin that performs either input or output functions. • A status pin that provides an LED that indicates a receive packet has passed address recognition. <p>This pin can also be controlled by PME_Enable bit (Func0_HwOptions<3>) in the serial ROM to be a wake-up event pin¹ that can be connected to pin pme# of the PCI connector or pin ctschg of the CardBus connector. When this pin is in a wake function, bit MiscHwOptions<1> in the serial ROM determines the polarity. The PME function takes precedence over the Magic Packet indication function. When the 21143 is in remote wake-up-LAN mode, this pin is used as an indicator that a Magic Packet has been successfully detected.</p>

Table 4 Functional Description of 21143 Signals

(Sheet 5 of 11)

Signal	Pin Type	Pin Number	Description
gep<3>/link	I/O	103	<p>This pin can be configured by software to be:</p> <ul style="list-style-type: none"> • A general-purpose pin that performs either input or output functions.² • A status pin that provides an LED to indicate: <ul style="list-style-type: none"> –Network link integrity state for 10BASE-T or 100BASE-TX.³ –Both network activity and network link integrity state.¹ • An input link status pin for OnNow support. When used with an MII PHY device, this pin should be connected to the MII PHY link indication pin (the 21143 interprets link-pass when this pin is high).¹ This pin should not be left unconnected.
gnt_l	I	21	Bus grant asserts to indicate to the 21143 that access to the bus is granted.
idsel	I	34	Initialization device select asserts to indicate that the host is issuing a configuration cycle to the 21143.
int_l	O/D	15	<p>Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. Interrupt request deasserts by writing a 1 into the appropriate CSR5 bit.</p> <p>If more than one interrupt bit is asserted in CSR5 and the host does not clear all input bits, the 21143 deasserts int_l for one cycle to support edge-triggered systems.</p>
iref	I	108	Current reference input for the analog phase-locked loop logic.
irdy_l	I/O	51	<p>Initiator ready indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of the clock when both irdy_l and target ready trdy_l are asserted. Wait cycles are inserted until both irdy_l and trdy_l are asserted together.</p> <p>When the 21143 is the bus master, it asserts irdy_l during write operations to indicate that valid data is present on the 32-bit ad lines. During read operations, the 21143 asserts irdy_l to indicate that it is ready to accept data.</p>

Signal Reference Tables

Table 4 Functional Description of 21143 Signals

(Sheet 6 of 11)

Signal	Type	Pin Number	Description
mii_clsn/sym_rxd<4>	I	118	In MII mode (CSR6<18>=1, CSR6<23>=0), this pin functions as the collision detect. When the external physical layer protocol (PHY) device detects a collision, it asserts this pin. In SYM mode (CSR6<18>=1, CSR6<23>=1), this pin functions as receive data. This line along with the four receive lines (sym_rxd<4:0>) provides five parallel data lines in symbol form. This data is controlled by an external physical layer medium-dependent (PMD) device and should be synchronized to the sym_rclk signal.
mii_crs/sd	I	117	In MII mode this pin functions as the carrier sense and is asserted by the PHY when the media is active. In SYM mode this pin functions as the signal detect indication. It is controlled by an external PMD device.
mii_dv	I	129	Data valid is asserted by an external PHY when receive data is present on the mii_rxd lines and is deasserted at the end of the packet. This signal should be synchronized with the mii_rclk signal.
mii_mdc	O	134	MII management data clock is sourced by the 21143 to the PHY devices as a timing reference for the transfer of information on the mii_mdio signal.
mii_mdio	I/O	135	MII management data input/output transfers control information and status between the PHY and the 21143.
mii/sym_rclk	I	128	Supports either the 25-MHz or 2.5-MHz receive clock. This clock is recovered by the PHY.

Table 4 Functional Description of 21143 Signals

(Sheet 7 of 11)

Signal	Type	Pin Number	Description
mii_rx_err/sel10_100	I/O	127	When used with an MII PHY device ($CSR6<18>=1$, $CSR6<23>=0$), this pin functions as receive error input. It is asserted when a data decoding error is detected by an external PHY device. This signal is synchronized to mii_rclk and can be asserted for a minimum of one receive clock. When asserted during a packet reception, it sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0). When used with a SYM PHY device ($CSR6<23>=1$), this pin functions as select 10/100 output. The signal sel10_100 equals 1 when the 21143 is in 100-Mb/s SYM mode ($CSR6<18>=1$) and equals 0 when the 21143 is in 10BASE-T/AUI mode ($CSR6<18>=0$).
mii/sym_rxd<3:0>	I	130, 131, 132, 133,	Four parallel receive data lines. This data is driven by an external PHY that attached the media and should be synchronized with the mii_rclk signal.
mii/sym_tclk	I	124	Supports the 25-MHz or 2.5-MHz transmit clock supplied by the external PMD device. This clock should always be active.
mii/sym_txd<3:0>	O	119, 120, 121, 122	Four parallel transmit data lines. This data is synchronized to the assertion of the mii_tclk signal and is latched by the external PHY on the rising edge of the mii_tclk signal.
mii_txen/sym_txd<4>	O	123	In MII mode, this pin functions as transmit enable. It indicates that a transmission is active on the MII port to an external PHY device. In SYM mode, this pin functions as transmit data. This line along with the four data transmit lines (sym_txd<3:0>) provides five parallel data lines in symbol form. The data is synchronized to the rising edge of the sym_tclk signal.
par	I/O	59	Parity is calculated by the 21143 as an even parity bit for the 32-bit ad and 4-bit c_be_1 lines. During address and data phases, parity is calculated on all the ad and c_be_1 lines whether or not any of these lines carry meaningful information.

Signal Reference Tables

Table 4 Functional Description of 21143 Signals

(Sheet 8 of 11)

Signal	Type	Pin Number	Description
pci_clk	I	19	The clock provides the timing for the 21143 related PCI bus transactions. All the bus signals are sampled on the rising edge of pci_clk . The clock frequency range is between 20 MHz and 33 MHz.
perr_l	I/O	57	Parity error asserts when a data parity error is detected. When the 21143 is the bus master and a parity error is detected, the 21143 asserts both CSR5 bit 13 (fatal bus error) and CFCS bit 24 (data parity report). Next, it completes the current data burst transaction, then stops operation. After the host clears the system error, the 21143 continues its operation. The 21143 asserts perr_l when a data parity error is detected in either a master-read or a slave-write operation.
req_l	O	22	Bus request is asserted by the 21143 to indicate to the bus arbiter that it wants to use the bus.
rst_l	I	16	Resets the 21143 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI output pins are put into tristate and all PCI O/D signals are floated.
serr_l	O/D	58	If an address parity error is detected and CFCS bit 8 (serr_l enable) is enabled, 21143 asserts both serr_l (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address.
sr_ck	O	114	Serial ROM clock signal. This pin provides a serial clock output for the serial ROM.
sr_cs	O	115	Serial ROM chip-select signal. This pin provides a chip select for the serial ROM.
sr_di	O	113	Serial ROM data-in signal. This pin serially shifts the write data from the 21143 to the serial ROM device.
sr_do	I	112	Serial ROM data-out signal. This pin serially shifts the read data from the serial ROM device to the 21143.

Table 4 Functional Description of 21143 Signals

(Sheet 9 of 11)

Signal	Type	Pin Number	Description
stop_I	I/O	56	Stop indicator indicates that the current target is requesting the bus master to stop the current transaction. The 21143 responds to the assertion of stop_I when it is the bus master, either to disconnect, retry, or abort.
tck	I	11	JTAG clock shifts state information and test data into and out of the 21143 during JTAG test operations. If the JTAG port is unused, this pin should be connected to vss .
tdi	I	13	JTAG data in is used to serially shift test data and instructions into the 21143 during JTAG test operations.
tdo	O	14	JTAG data out is used to serially shift test data and instructions out of the 21143 during JTAG test operations.
tms	I	12	JTAG test mode select controls the state operation of JTAG testing in the 21143.
tp_rd-	I	10	Twisted-pair negative differential receive data from the twisted-pair lines.
tp_rd+	I	9	Twisted-pair positive differential receive data from the twisted-pair lines.
tp_td-	O	5	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td- -	O	4	
tp_td+	O	6	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are combined resistively outside the 21143 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ +	O	7	

Signal Reference Tables

Table 4 Functional Description of 21143 Signals

(Sheet 10 of 11)

Signal	Type	Pin Number	Description
trdy_1	I/O	52	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both trdy_1 and irdy_1 are asserted. Wait cycles are inserted until both irdy_1 and trdy_1 are asserted together. When the 21143 is the bus master, target ready is asserted by the bus slave on the read operation, which indicates that valid data is present on the ad lines. During a write cycle, it indicates that the target is prepared to accept data.
vcap_h	I	110	Capacitor input for analog phase-locked loop logic.
vdd	P	1, 2, 8, 18, 26, 36, 37, 46, 54, 67, 72, 73, 79, 95, 107, 125, 136, 141	3.3-V supply input. These pins should be connected to the auxiliary power, if such power exists. Otherwise, these pins should be connected to the main power.
vddac	P	109, 111	Supplies +3.3-V input for analog phase-locked loop logic.
vdd_clamp	P	20	Supplies +5-V or +3.3-V reference for clamp logic. This pin is also used to identify the lack of main power when the auxiliary power is on. This pin should be connected to the main power.
vss	P	3, 17, 30, 35, 38, 42, 53, 63, 71, 74, 83, 94, 104, 116, 126, 144	Ground pins.

Table 4 Functional Description of 21143 Signals

(Sheet 11 of 11)

Signal	Type	Pin	Description
		Number	
xtal1	I	106	20-MHz crystal input, or crystal oscillator input.
xtal2	O	105	Crystal feedback output pin used for crystal connections only. If this pin is unused, then it should be unconnected.

¹This feature is only supported in the 21143–PD and the 21143–TD.

²In the 21143–PD and the 21143–TD, when used as a general-purpose input pin, this pin affects the link changed wake-up event.

³The 100BASE-TX link indication feature is only supported in the 21143–PD and the 21143–TD.

Pin Tables

2.2 Pin Tables

This section contains four types of pin tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.
- Table 8 lists the open drain pins.

Table 5 Input Pins

Signal	Active Level	Signal	Active Level
au _i _cd ₋	Low	mii/sym_tclk	—
au _i _cd ₊	High	pci_clk	—
au _i _rd ₋	—	rst_l	Low
au _i _rd ₊	—	sr_do	—
gnt_l	Low	tck	—
idsel	High	tdi	—
iref	—	tms	—
mii_clsn/sym_rxd<4>	High for mii_clsn, — for sym_rxd<4>	tp_rd ₋	—
mii_crs/sd	High	tp_rd ₊	—
mii_dv	High	vcap_h	—
mii/sym_rclk	—	xtal1	—
mii/sym_rxd<3:0>	—	—	—

Table 6 Output Pins

Signal	Active Level	Signal	Active Level
au_i_td-	—	sr_ck	—
au_i_td+	—	sr_cs	High
br_a<0>/cb_pads_l	High for br_a<0>, low for cb_pads_l	sr_di	—
br_a<1>	High	tdo	—
br_ce_l	Low	tp_td-	—
mii_mdc	—	tp_td--	—
mii/sym_txd<3:0>	—	tp_td+	—
mii_txen/sym_txd<4>	High for mii_txen, — for sym_txd<4>	tp_td++	—
req_l	Low	xtal2	—

Table 7 Input/Output Pins

Signal	Active Level	Signal	Active Level
ad<31:0>	—	gep<3>/link	— for gep<3>, high for link
br_ad<7:0>	—	irdy_l	Low
clkrun_l	Low	mii_mdio	—
c_be_l<3:0>	Low	mii_rx_err/sel10_100	High for mii_rx_err, — for sel10_100
devsel_l	Low	par	—
frame_l	Low	perr_l	Low
gep<0>/au_i_bnc	—	stop_l	Low
gep<1>/activ	— for gep<1>, high for activ	trdy_l	Low
gep<2>/rev_match/wake	— for gep<2>, high for rev_match, — ¹ for wake	—	—

¹The active level is controlled by bit MiscHwOptions<1> (PME_STSCHG) in the serial ROM.

Signal Grouping by Function

Table 8 Open Drain Pins

Signal	Active Level	Signal	Active Level
int_1	Low	serr_1	Low

2.3 Signal Grouping by Function

Table 9 lists the signals according to their interface function.

Table 9 Signal Functions

(Sheet 1 of 3)

Interface	Function	Signals
PCI/CardBus	Address and data	ad<31:0>, par
	Arbitration	gnt_1, req_1
	Bus command and byte enable	c_be_1<3:0>
	Device select	devsel_1, idsel
	Error reporting	perr_1, serr_1
	Interrupt	int_1
	System	pci_clk, rst_1
	Control signals	frame_1, stop_1, irdy_1, trdy_1
	Power-management status	wake
	Clock status	clkrun_1
	Pad select	cb_pads_1
MII/SYM network port	Transmit data lines	mii/sym_txd<3:0>
	Receive data lines	mii/sym_rxd<3:0>
	Transmit, receive clocks	mii/sym_tclk, mii/sym_rclk
	Transmit enable	mii_txen
	Collision detect	mii_clsn
	MII error reporting	mii_rx_err
	Data control	mii_dv, mii_crs
	MII management data clock	mii_mdc

Signal Grouping by Function

Table 9 Signal Functions

(Sheet 2 of 3)

Interface	Function	Signals
	MII management data input/output	mii_mdio
	Signal detection	sd
	SYM mode data lines	sym_rxd<4>, sym_txd<4>
	SYM mode 10/100 select	sel10_100
Test access port	JTAG test operations	tck, tdi, tdo, tms
Serial ROM port	Serial ROM	sr_ck, sr_cs, sr_di, sr_do
Boot ROM port	ROM interface	br_a<1:0>, br_ad<7:0>, br_ce_l
Power	3.3-V or 5.0-V supply input	vdd_clamp
	3.3-V supply input	vdd, vddac
	Ground	vss
General-purpose port and LEDs	General-purpose pins	gcp<3:0>
	LED indicators	activ, rcv_match, link
	10BASE5/10BASE2 select	au_i_bnc
Network connection	Analog phase-locked loop logic	iref, vcap_h
	AUI collision data	au_i_cd-, au_i_cd+

Signal Grouping by Function

Table 9 Signal Functions

(Sheet 3 of 3)

Interface	Function	Signals
	AUI transmit and receive data	au_i_rd₋, au_i_rd₊, au_i_td₋, au_i_td₊
	Crystal oscillator	xtal1, xtal2
	Twisted-pair transmit and receive data	tp₋_rd₋, tp₋_rd₊, tp₋_td₋, tp₋_td₋ -, tp₋_td₊, tp₋_td₊ +

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications for the 21143.

Caution: Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21143. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21143.

3.1 Voltage Limit Ratings

Table 10 lists the voltage limit ratings.

Table 10 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	3.0 V	3.6 V
vdd_clamp (5.0 V)	4.75 V	5.25 V
vdd_clamp (3.3 V) ¹	3.0 V	3.6 V
ESD protection voltage	—	2000 V

¹In the 3.3-V signaling environment, **vdd_clamp** must not be greater than **vdd** + 0.3 V.

3.2 Temperature Limit Ratings

Table 11 lists the temperature limit ratings.

Table 11 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	-55°C (-67°F)	125°C (257°F)
Operating temperature	0°C (32°F)	70°C (158°F)

3.3 Power Specifications

This section describes the power specifications for all versions of the 21143 device.

PCI Bus and CardBus Electrical Parameters

3.3.1 21143–PB through 21143–TC Power Specifications

The values in Table 12 are based on a PCI or CardBus clock frequency of 33 MHz and a network data rate of 10/100 Mb/s for MII for the 21143–PB, 21143–TB, 21143–PC, and the 21143–TC.

Table 12 21143–PB to 21143–TC Power Specifications

Mode	IDD ¹ (mA)	Power ¹ (mW)	IDD ² (mA)	Power ² (mW)
After power-up	54	178	—	—
Normal	150	495	230	828
Snooze	85	280	145	522
Sleep	25	82	115	414

¹Typical: **vdd** = 3.3 V, Ta = 25°C

²Maximum: **vdd** = 3.6 V, Ta = 0°C

3.3.2 21143–PD and 21143–TD Power Specifications

The values in Table 13 are based on a PCI or CardBus clock frequency of 33 MHz, **vdd** at 3.6 V, Ta at 0°C, and a network data rate of 10/100 Mb/s for MII for the 21143–PD and the 21143–TD.

Table 13 21143–PD and 21143–TD Power Specifications

Condition	Typical Power with Idle Activity (mW)	Typical Power with Full Activity (mW)
D0 in snooze mode ¹	TBD	TBD
D1 in snooze mode	TBD	TBD
D2 or D3 mode	TBD ²	TBD ³
After power-up ⁴	TBD	—
Normal mode	—	TBD

¹The D0 in snooze mode is equivalent to the traditional snooze mode.

²PCI/CardBus clock is stopped.

³PCI/CardBus clock is running.

⁴After power-up, the 21143 is in the sleep mode.

3.4 PCI Bus and CardBus Electrical Parameters

This section describes the PCI Bus and CardBus characteristics for the 21143.

3.4.1 PCI and CardBus I/O Voltage Specifications

The 21143 meets the I/O voltage specifications listed in Table 14 and Table 15.

Table 14 I/O Voltage Specifications for 5.0-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	2.0 V	vdd_clamp + 0.5 V
V_{il}	Input low voltage	—	-0.5 V	0.8 V
I_i^1	Input leakage current	$0.5\text{ V} < V_{in} < 2.7\text{ V}$	—	$\pm 10\ \mu\text{A}$
V_{oh}	Output high voltage	$I_{out} = -2\text{ mA}$	2.4 V	—
V_{ol}^2	Output low voltage	$I_{out} = 3\text{ mA}, 6\text{ mA}$	—	0.55 V
Cap^3	Pin capacitance	—	5 pF	8 pF

¹Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

²Signals without pull-up resistors must have 3-mA low output current. Signals requiring pull-up resistors (including **frame_1**, **trdy_1**, **irdy_1**, **devsel_1**, **stop_1**, **serr_1**, and **perr_1**) must have 6 mA.

³Parameter design guarantee.

Table 15 I/O Voltage Specifications for 3.3-V Levels

Symbol	Parameter	Condition	Minimum	Maximum
V_{ih}	Input high voltage	—	$0.475 * \mathbf{vdd_clamp}$	vdd_clamp + 0.5 V
V_{il}	Input low voltage	—	-0.5 V	$0.325 * \mathbf{vdd_clamp}$
I_i^1	Input leakage current	$0.0\text{ V} < V_{in} < \mathbf{vdd_clamp}$	—	$\pm 70\ \mu\text{A}$
V_{oh}	Output high voltage	$I_{out} = -500\ \mu\text{A}$	$0.9 * \mathbf{vdd_clamp}$	—
V_{ol}	Output low voltage	$I_{out} = 1500\ \mu\text{A}$	—	$0.1 * \mathbf{vdd_clamp}$
Cap^2	Pin capacitance	—	5 pF	8 pF

¹Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

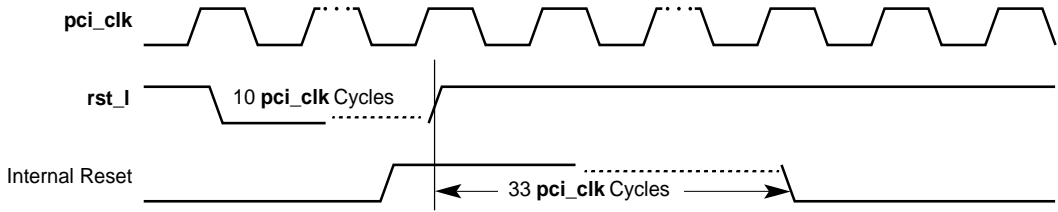
²Parameter design guarantee.

PCI Bus and CardBus Electrical Parameters

3.4.2 System Bus Reset

System bus (PCI or CardBus) reset (**rst_1**) is an asynchronous signal that must be active for at least 10 system bus (PCI or CardBus) clock (**pci_clk**) cycles. Figure 3 shows the reset timing characteristics, and Table 16 lists the reset signal limits.

Figure 3 Reset Timing Diagram



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Table 16 Reset Timing Parameters

Symbol	Parameter	Minimum	Maximum	Condition
Trst	rst_1 pulse width	10* pci_clk	Not applicable	pci_clk active

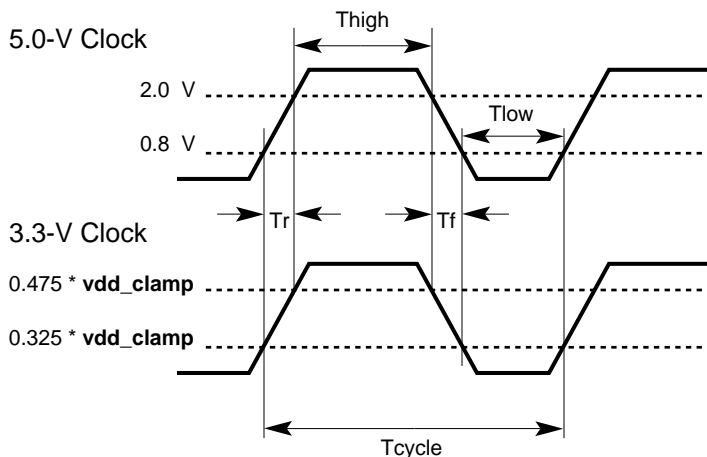
3.4.3 PCI and CardBus Clock Specifications

The clock frequency range¹ for PCI and CardBus is between 20 MHz and 33 MHz. Figure 4 shows the PCI and CardBus clock specification timing characteristics and the required measurement points for both the 5.0-V and 3.3-V signaling environments. Table 17 lists the frequency-derived clock specifications.

¹The PCI and CardBus clock frequency is from dc to 33 MHz; network operational with the PCI or CardBus clock from 20 MHz to 33 MHz.

PCI Bus and CardBus Electrical Parameters

Figure 4 PCI and CardBus Clock Specification Timing Diagram



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Table 17 PCI and CardBus Clock Timing Specifications

Symbol	Parameter	Minimum	Maximum
T_{cycle}	Cycle time	30 ns	50 ns
T_{high}	pci_clk high time	11 ns	—
T_{low}	pci_clk low time	11 ns	—
T_r/T_f^1	pci_clk slew rate	1 V/ns	4 V/ns

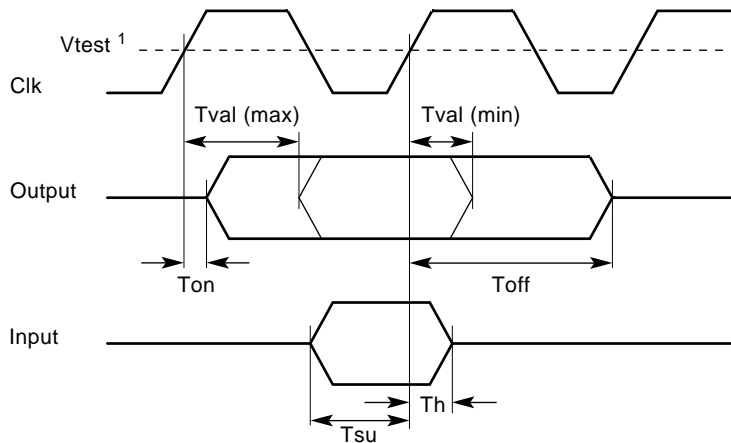
¹Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.4.4 Other PCI and CardBus Signals

Figure 5 shows the timing diagram characteristics for other PCI and CardBus signals and Table 18 lists their timing specifications. This timing is identical to the timing for the general-purpose register signals.

PCI Bus and CardBus Electrical Parameters

Figure 5 Timing Diagram for Other PCI and CardBus Signals



¹ Vtest is 1.5 V in a 5.0-V signaling environment and is $0.4 * \text{vdd_clamp}$ in a 3.3-V signaling environment.

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Table 18 Other PCI and CardBus Signals' Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tval ¹	clk-to-signal valid delay	2 ns	11 ns
Ton ²	Float-to-active delay from clk	2 ns	—
Toff ²	Active-to-float delay from clk	—	28 ns
Tsu	Input signal valid setup time before clk	7 ns	—
Th	Input signal hold time from clk	0 ns	—
Slewr, Slew ^{f2}	Output rise and fall slew rate ³	1 V/ns	4 V/ns
Slewr, Slew ^{f2}	Output rise and fall slew rate ⁴	0.25 V/ns	1 V/ns

¹Load for this measurement is as specified in *PCI Local Bus Specification*, Revision 2.0 and *PCI Local Bus Specification*, Revision 2.1.

²Parameter design guarantee.

³Slew rate for PCI, selected by default when pin **cb_pad_1** is not pulled down externally.

⁴Slew rate for CardBus, selected when pin **cb_pad_1** is pulled down externally.

3.5 AUI and Twisted-Pair DC Specifications

Table 19 lists the dc specifications for the AUI and twisted-pair parts of the SIA.

Table 19 AUI and Twisted-Pair DC Specifications

Symbol	Definition	Condition	Minimum	Maximum	Unit
AUI Pins					
V_{od}	Transmit differential output voltage (au_i_td±)	78 Ω termination	± 550	± 1200	mV
V_{odi}^1	Transmit differential output idle voltage (au_i_td±)	78 Ω termination	-40	+40	mV
I_{odi}^1	Transmit differential output idle current (au_i_td±)	78 Ω termination	-1	+1	mA
V_{asq}^{+1}	Differential positive squelch threshold (au_rd±)	—	175	275	mV
V_{asq}^{-1}	Differential negative squelch threshold (au_rd± and au_cd±)	—	-275	-175	mV
V_{odu}^1	Transmit differential output undershoot voltage on return to zero (au_i_td±)	78 Ω termination	—	-100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (tp_td± and tp_td±±)	$I_{oh} = -25$ mA	2.5	—	V
V_{tol}	Output low voltage (tp_td± and tp_td±±)	$I_{ol} = 25$ mA	—	0.5	V
V_{tsq}^{+1}	Differential positive squelch threshold (tp_rd±)	—	300	520	mV
V_{tsq}^{-1}	Differential negative squelch threshold (tp_rd±)	—	-520	-300	mV
V_{tdif}^1	Differential input voltage range (tp_rd±)	—	-3.1	3.1	V

¹Parameter design guarantee.

Serial Interface Attachment Specifications

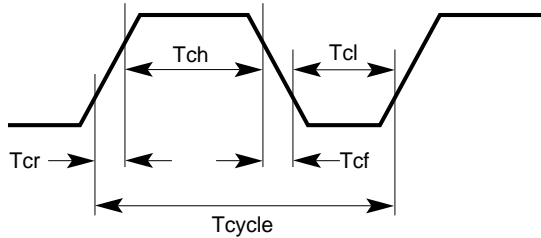
3.6 Serial Interface Attachment Specifications

This section describes the dc specifications and timing limits of the SIA unit.

3.6.1 Serial Clock Timing

Figure 6 shows the serial clock (TTL or CMOS) timing characteristics, and Table 20 lists the serial clock timing specifications.

Figure 6 Serial Clock (XTAL) Timing Diagram



LJ-04101.A14

Table 20 Serial Clock (XTAL) Timing Specifications

Symbol	Parameter	Minimum	Maximum
T_{cr}^1	Rise time	—	4 ns
T_{cf}^1	Fall time	—	4 ns
T_{cycle}^1	Cycle time	49.995 ns	50.005 ns
T_{ch}	Clock high time	$0.4 * T_{cycle}$	$0.6 * T_{cycle}$
T_{cl}	Clock low time	$0.4 * T_{cycle}$	$0.6 * T_{cycle}$

¹Parameter design guarantee.

Serial Interface Attachment Specifications

3.6.2 Internal SIA Mode AUI Timing—Transmit

Figure 7 shows the internal SIA transmit timing characteristics for the AUI, and Table 21 lists the internal SIA transmit timing limits for the AUI.

Figure 7 Internal SIA Mode AUI Timing Diagram—Transmit

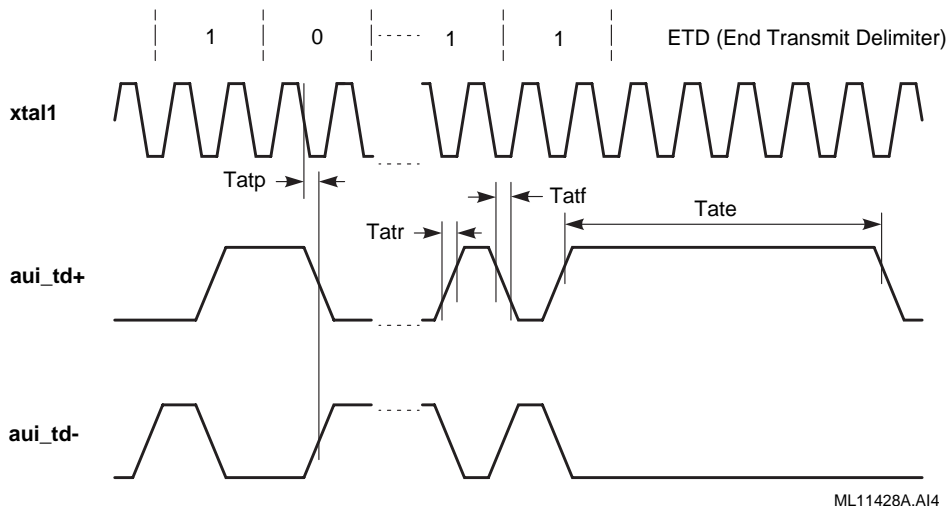


Table 21 Internal SIA Mode AUI Timing Specifications—Transmit

Symbol	Definition	Minimum	Maximum	Unit
Tatp	aui_td+ , aui_td- propagation delay from xtal1 fall	—	30	ns
Tatr ¹	aui_td+ , aui_td- rise time	2	8	ns
Tatf ¹	aui_td+ , aui_td- fall time	2	8	ns
Tatm ¹	aui_td+ , aui_td- rise and fall time mismatch (not shown)	—	1	ns
Tate ¹	aui_td± end transmit delimiter length	345	405	ns

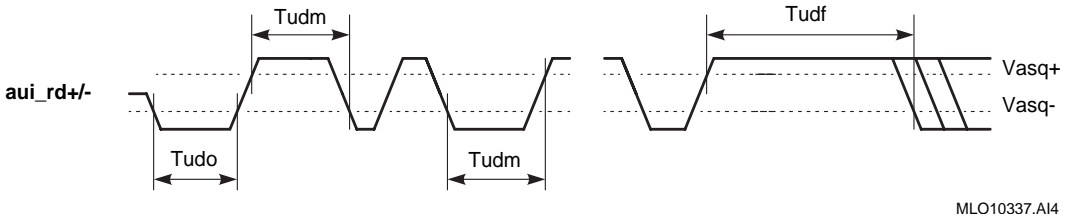
¹Parameter design guarantee.

Serial Interface Attachment Specifications

3.6.3 Internal SIA Mode AUI Timing—Receive

Figure 8 shows the internal SIA receive timing characteristics for the AUI, and Table 22 lists the internal SIA receive timing limits for the AUI.

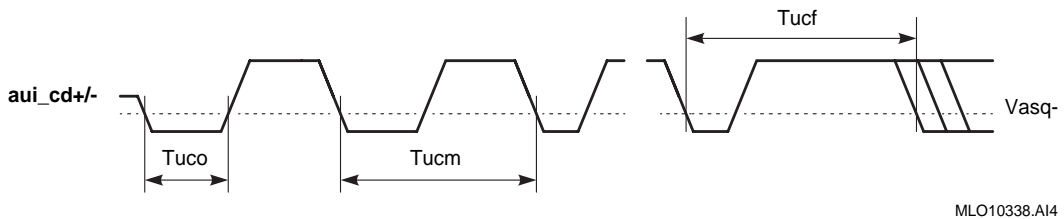
Figure 8 Internal SIA Mode AUI Timing Diagram—Receive



3.6.4 Internal SIA Mode AUI Timing—Collision

Figure 9 shows the internal SIA collision timing characteristics for the AUI, and Table 22 lists the internal SIA collision timing limits for the AUI.

Figure 9 Internal SIA Mode AUI Timing Diagram—Collision



Serial Interface Attachment Specifications

Table 22 Internal SIA Mode AUI Timing Specifications—Receive and Collision

Symbol	Definition	Minimum	Maximum	Unit
Tudo	au_i_rd ± start of frame pulse width	15	20	ns
Tudm ¹	au_i_rd ± delay between opposite squelch crossings not recognized as end of packet	—	140	ns
Tudf ¹	au_i_rd ± delay from last squelch crossing recognized as end of packet	150	—	ns
Tuco	au_i_cd ± start of collision pulse width	20	25	ns
Tucm ¹	au_i_cd ± delay between squelch crossings not recognized as end of collision	—	140	ns
Tucf ¹	au_i_cd ± delay from last squelch crossing recognized as end of collision	150	—	ns

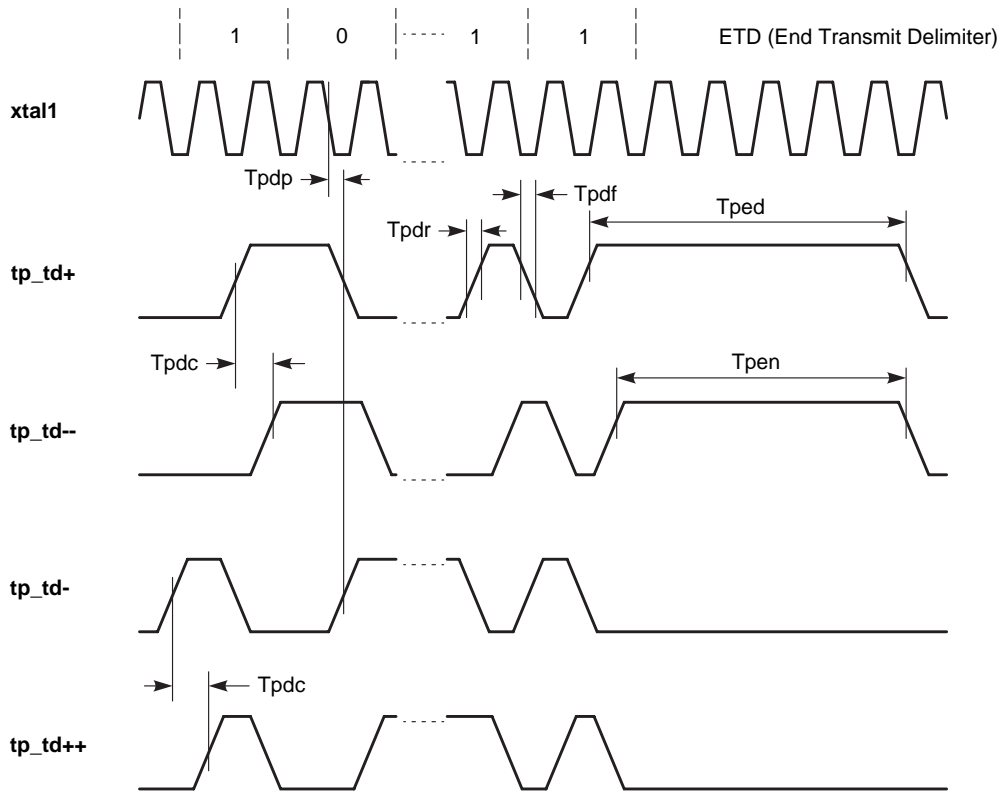
¹Parameter design guarantee.

3.6.5 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA transmit limits.

Serial Interface Attachment Specifications

Figure 10 Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit



ML11429A.AI4

Table 23 Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit

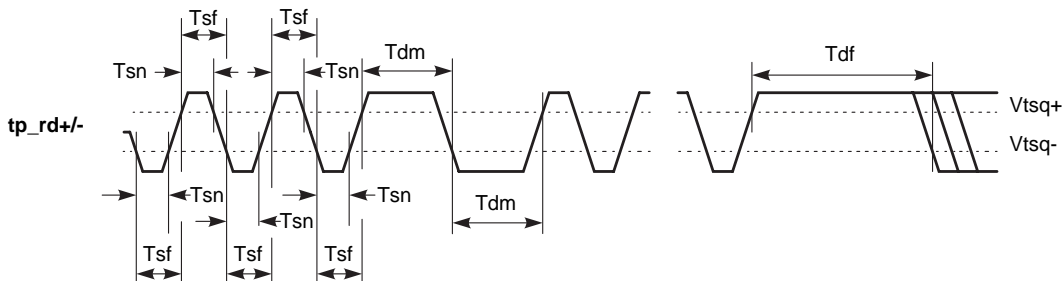
Symbol	Definition	Minimum	Maximum	Unit
T_{pdp}	tp_td+ , tp_td- propagation delay from $xtall1$ fall	—	30	ns
T_{pdr}^1	tp_td+ , tp_td++ , tp_td- , tp_td- – rise time	2	8	ns
T_{pdf}^1	tp_td+ , tp_td++ , tp_td- , tp_td- – fall time	2	8	ns
T_{pdm}^1	tp_td+ , tp_td++ , tp_td- , tp_td- – rise and fall time mismatch (not shown)	—	1	ns
T_{pdc}^1	tp_td+ to tp_td- – and tp_td- to tp_td++ delay	46	54	ns
T_{ped}^1	$tp_td\pm$ end transmit delimiter length	295	355	ns
T_{pen}^1	$tp_td++/-$ – end transmit delimiter length	245	305	ns

¹Parameter design guarantee.

3.6.6 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 11 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive



MLO10340.A4

Table 24 Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive

Symbol	Definition	Minimum	Maximum	Unit
T_{sn}^1	$tp_{rd\pm}$ start of frame pulse width during smart squelch operation	15	20	ns
T_{sf}^1	$tp_{rd\pm}$ maximum delay between opposite squelch crossings not to turn smart squelch off	140	150	ns
T_{dm}^1	$tp_{rd\pm}$ delay between opposite squelch crossings not recognized as end of packet	—	140	ns
T_{df}^1	$tp_{rd\pm}$ delay from last squelch crossing recognized as end of packet	150	—	ns

¹Parameter design guarantee.

Serial Interface Attachment Specifications

3.6.7 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 12 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 25 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 12 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

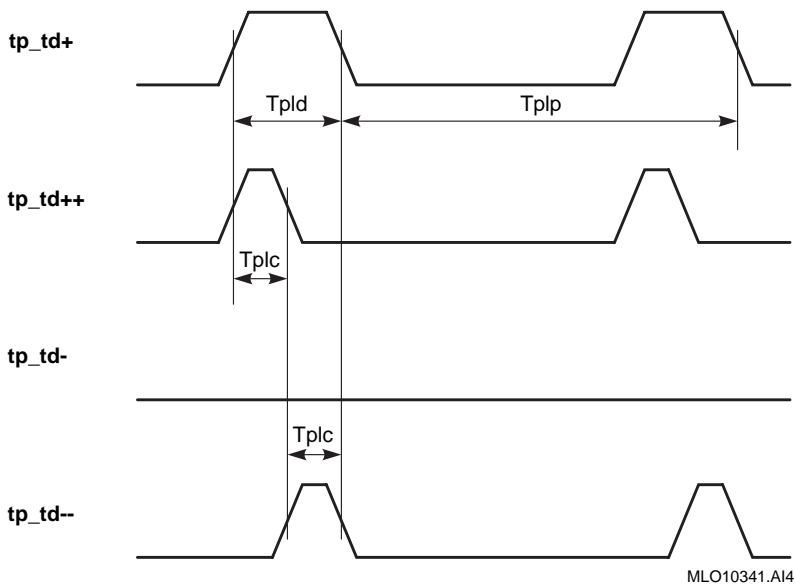


Table 25 Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Unit
$Tpld^1$	tp_td+ idle link pulse width	80	120	ns
$Tplc^1$	tp_td++ and tp_td-- idle link pulse width	40	60	ns
$Tplp^1$	Idle link pulse period	8	24	ms

¹Parameter design guarantee.

3.7 MII Interface Specifications

Table 26 lists the specifications for the MII interface.

Table 26 MII Interface

Symbol	Definition	Condition	Minimum	Maximum	Unit
V_{oh}	Output high voltage	$I_{oh} = -4 \text{ mA}$	2.4	—	V
V_{ol}	Output low voltage	$I_{ol} = 4 \text{ mA}$	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{in}	Input current	$V_{in} = \text{vcc or vss}$	-10.0	10.0	μA
I_{oz}	Maximum tristate output leakage current	$V_{in} = \text{vdd or vss}$	-10.0	10.0	μA

3.8 MII/SYM Port Timing

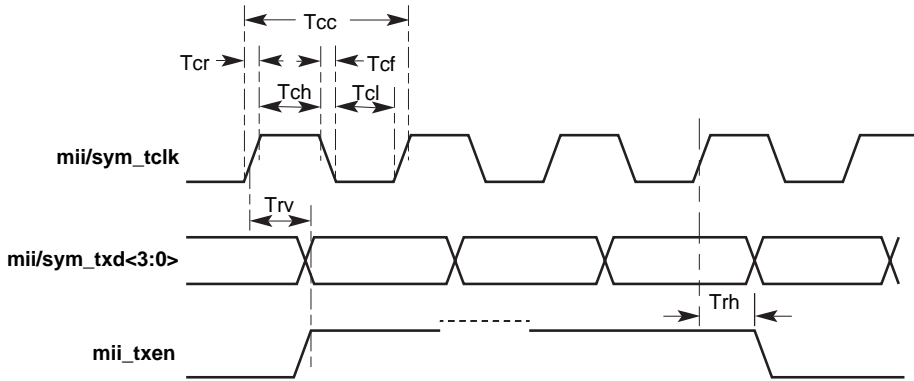
This section describes the MII/SYM port timing limits.

3.8.1 MII/SYM 10/100-Mb/s and 10-Mb/s Timing—Transmit

Figure 13 shows the MII/SYM port transmit timing characteristics, and Table 27 lists the MII/SYM port transmit timing limits.

MII/SYM Port Timing

Figure 13 MII/SYM Port Timing Diagram—Transmit



LJ-04944.A14

Table 27 MII/SYM Port Timing Limits—Transmit

Symbol	Definition	Minimum	Typical	Maximum	Unit
Tcc ¹	mii/sym_tclk cycle	—	40t ⁴	—	ns
Tch	mii/sym_tclk high time	14t ⁴	—	26t ⁴	ns
Tcl	mii/sym_tclk low time	14t ⁴	—	26t ⁴	ns
Tcr ²	mii/sym_tclk rise time	—	8	—	ns
Tcf ²	mii/sym_tclk fall time	—	8	—	ns
Trv ³	mii_tclk rise to mii_txen valid time or mii/sym_tclk rise to mii/sym_txd valid time	—	—	20	ns
Trh	mii_txen hold after mii_telk rise time	5	—	—	ns

¹±50 parts per million.

²Parameter design guarantee.

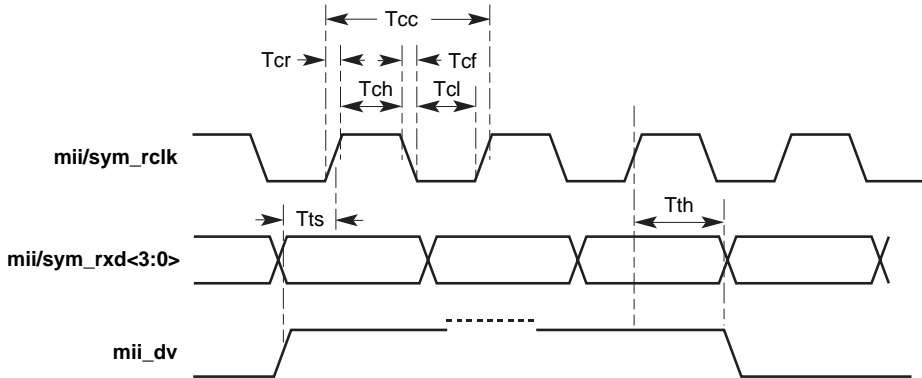
³The transmit data (**mii/sym_txd**) and transmit enable (**mii_txen**) output pins are driven internally from the rising edge of **mii/sym_tclk**.

⁴t=1 for 100-Mb/s operation; t=10 for 10-Mb/s operation.

3.8.2 MII/SYM 10/100-Mb/s Timing—Receive

Figure 14 shows the MII/SYM port receive timing characteristics, and Table 28 lists the MII/SYM port receive timing limits.

Figure 14 MII/SYM Port Timing Diagram—Receive



LJ-04998.A14

Table 28 MII/SYM Port Timing Limits—Receive

Symbol	Definition	Minimum	Typical	Maximum	Unit
T_{cc}^1	mii/sym_rclk cycle time	—	$40t^4$	—	ns
T_c	mii/sym_rclk high time	$14t^4$	—	$26t^4$	ns
T_{cl}	mii/sym_rclk low time	$14t^4$	—	$26t^4$	ns
T_{cr}^2	mii/sym_rclk rise time	—	8	—	ns
T_{cf}^2	mii/sym_rclk fall time	—	8	—	ns
T_{ts}^3	mii/sym_rxd setup (both rise and fall transactions) to mii/sym_rclk rise time or mii_dv setup (both rise and fall transactions) to mii_rclk rise time	8	—	—	ns
T_{th}	mii/sym_rxd hold (both rise and fall transactions) after mii/sym_rclk rise time or mii_dv hold (both rise and fall transactions) after mii_rclk rise time	10	—	—	ns

¹ ± 50 parts per million.

²Parameter design guarantee.

³The receive data (**mii/sym_rxd**) and data valid (**mii_dv**) input pins are latched internally on the rising edge of **mii/sym_rclk**.

⁴ $t=1$ for 100-Mb/s operation; $t=10$ for 10-Mb/s operation.

MII/SYM Port Timing

3.8.3 SYM 10/100-Mb/s Timing—Signal Detect

Figure 15 shows the SYM port signal detect timing characteristics, and Table 29 lists the SYM port signal detect timing limits.

Figure 15 SYM Port Timing Diagram—Signal Detect

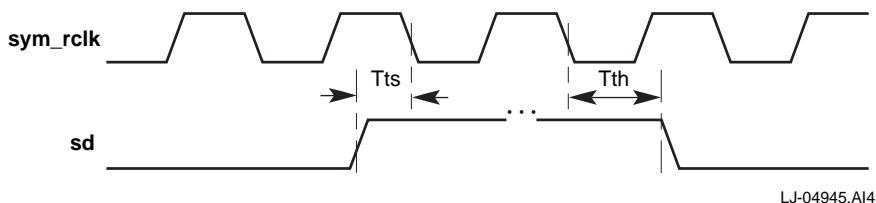


Table 29 SYM Port Timing Limits—Signal Detect

Symbol	Definition	Minimum	Maximum	Units
T_{ts}^1	sd setup (both rise and fall transactions) to sym_rclk fall time	10	—	ns
T_{th}^1	sd hold (both rise and fall transactions) after sym_rclk fall time	12	—	ns

¹Input signal detect (**sd**) is latched internally on the falling edge of **sym_rclk**.

3.8.4 MII 10/100-Mb/s Timing—Receive Error

Figure 16 shows the MII port receive error timing characteristics, and Table 30 lists the MII port receive error timing limits.

Figure 16 MII Port Timing Diagram—Receive Error

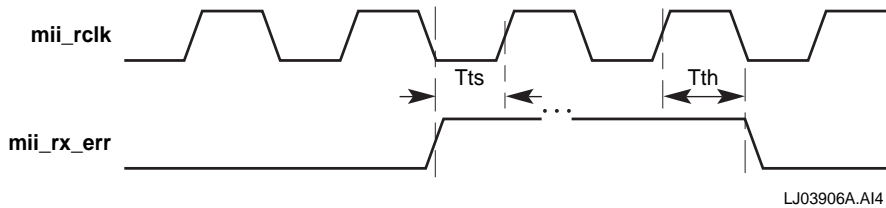


Table 30 MII Port Timing Limits—Receive Error

Symbol	Definition	Minimum	Maximum	Unit
T_{ts}^1	mii_rx_err setup (both rise and fall transactions) to mii_rclk rise time	10	—	ns
T_{th}^1	mii_rx_err hold (both rise and fall transactions) after mii_rclk rise time	10	—	ns

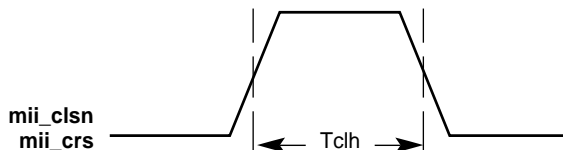
¹Input signal detect (**mii_rx_err**) is latched internally on the falling edge of **mii_rclk**.

Boot ROM and Serial ROM Port Specification

3.8.5 MII 10/100-Mb/s Timing—Carrier Sense and Collision

Figure 17 shows the MII port carrier sense and collision timing characteristics, and Table 31 lists the MII port carrier sense and collision timing limits.

Figure 17 MII Port Timing Diagram—Carrier Sense and Collision



LJ-03929.A14

Table 31 MII Port Timing Limits—Carrier Sense and Collision

Symbol	Definition	Minimum	Maximum	Unit
Tchl	mii_crs, mii_clsn high time	20	—	ns

3.9 Boot ROM and Serial ROM Port Specification

Table 32 lists the dc specifications for the boot ROM and serial ROM ports. These specifications apply in any mode in which the ports are used.

Table 32 Boot ROM and Serial ROM Port DC Specifications

Symbol	Definition	Condition	Minimum	Maximum	Unit
V_{oh}	Output high voltage	$I_{oh} = -4$ mA	2.4	—	V
V_{ol}	Output low voltage	$I_{ol} = 4$ mA	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{oz}^1	Maximum tristate output leakage current	$V_{out} = \mathbf{vdd}$ or \mathbf{vss}	-10	10	μA

¹For **sr_do** and **br_ce_1**, the maximum value is 1000.0 μA .

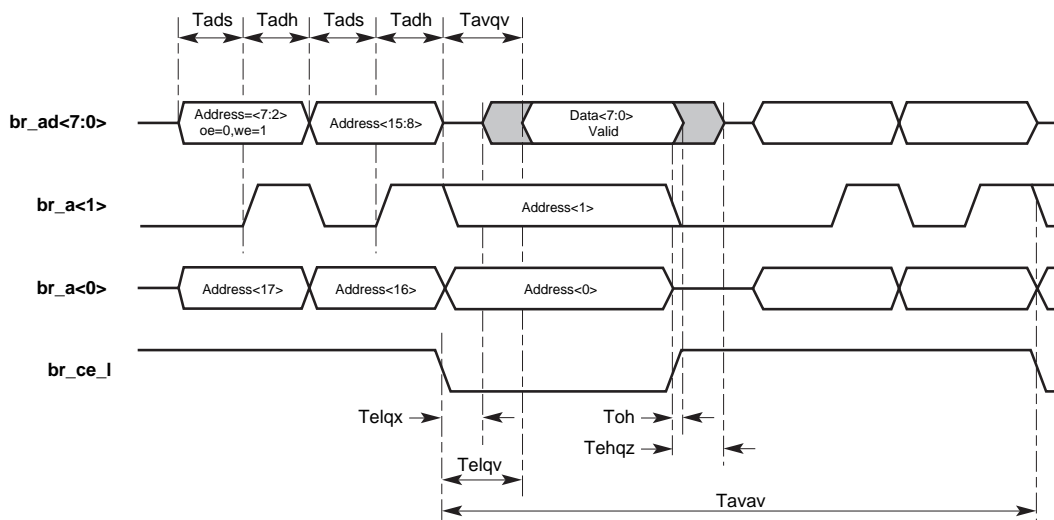
3.10 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.10.1 Boot ROM Read Timing

Figure 18 shows the boot ROM read timing characteristics, and Table 33 lists the boot ROM read timing limits.

Figure 18 Boot ROM Read Timing Diagram



LJ-04941.A14

Table 33 Boot ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
Tavav	Read cycle time	240	—	ns
Tavqv	Address to output delay	—	240	ns
Telqv	br_ce_1 to output delay	—	240	ns
Telqx ¹	br_ce_1 to output low impedance	0	—	ns
Tehqz ¹	br_ce_1 going high to output high impedance	—	55	ns
Toh	Output hold from br_ce_1 change	0	—	ns
Tads	Address setup to latch enable high	30	—	ns
Tadh	Address hold from latch enable high	30	—	ns

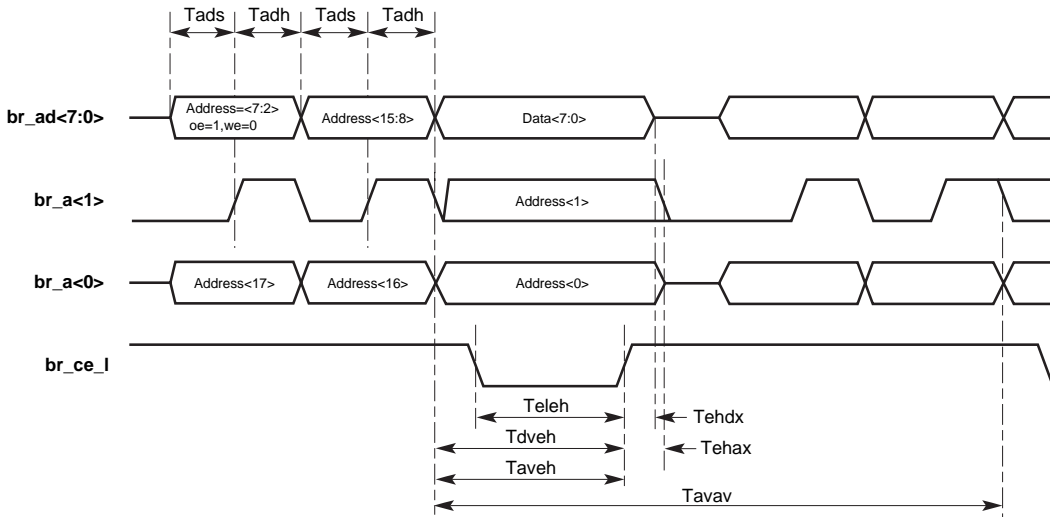
¹Parameter design guarantee.

Boot ROM Port Timing

3.10.2 Boot ROM Write Timing

Figure 19 shows the boot ROM write timing characteristics, and Table 34 lists the boot ROM write timing limits.

Figure 19 Boot ROM Write Timing Diagram



LJ-04999.AI4

Table 34 Boot ROM Write Timing Specifications

Symbol ¹	Parameter	Minimum	Unit
Tavav	Write cycle time	240	ns
Teleh	br_ce_1 pulse width	70	ns
Taveh	Address setup to br_ce_1 going high	50	ns
Tdveh	Data setup to br_ce_1 going high	50	ns
Tehdx	Data hold from br_ce_1 going high	10	ns
Tehax	Address hold from br_ce_1 high	15	ns
Tads	Address setup to latch enable high	30	ns
Tadh	Address hold from latch enable high	30	ns

¹There are no maximum specifications.

3.11 Serial ROM Port Timing

Figure 20 shows the serial ROM port timing, and Table 35 lists the characteristics. This timing is identical to the timing for the MII management signals (**mii_mdio** and **mii_mdc**).

Figure 20 Serial ROM Port Timing Diagram

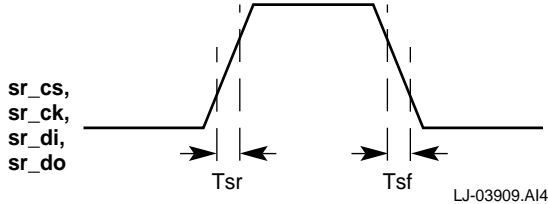


Table 35 Serial ROM Port Timing Characteristics

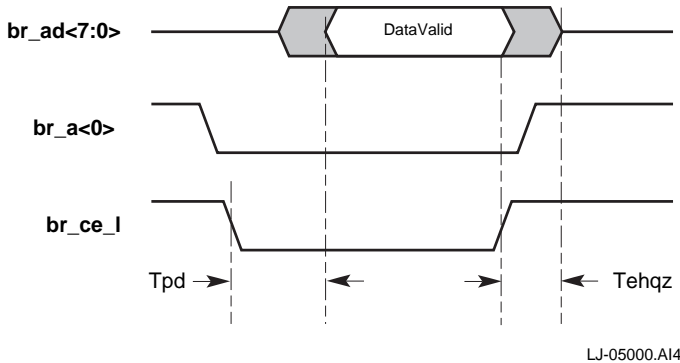
Symbol	Definition	Minimum	Maximum	Unit
T_{sr}^1	Rise time	—	10	ns
T_{sf}^1	Fall time	—	10	ns

¹Parameter design guarantee.

3.12 External Register Timing

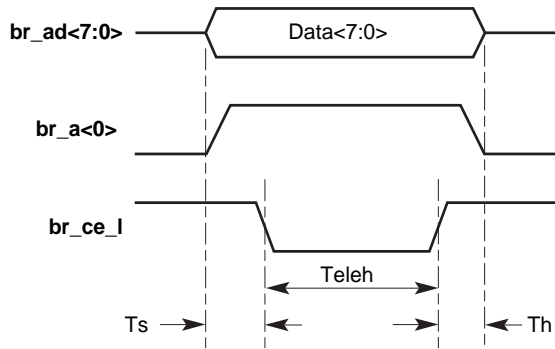
Figure 21 shows the external register read timing characteristics, and Figure 22 shows the write timing characteristics. Table 36 lists the external register timing specifications for both read and write operations.

Figure 21 External Register Read Timing Diagram



Joint Test Action Group—Test Access Port

Figure 22 External Register Write Timing Diagram



LJ-05001.AI4

Table 36 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
Teleh	br_ce_l pulse width	120	—	ns
Read Timing				
T_{pd}	br_ce_l low to br_ad<7:0> valid high	—	20	ns
Tehqz¹	br_ce_l high to br_ad<7:0> high impedance	—	20	ns
Write Timing				
T_s	Data setup time prior to br_ce_l	30	—	ns
T_h	Data hold after br_ce_l high	30	—	ns

¹Parameter design guarantee.

3.13 Joint Test Action Group—Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.13.1 JTAG DC Specifications

Table 37 lists the dc specifications for the JTAG pins.

Table 37 JTAG DC Specifications

Symbol	Definition	Condition	Minimum	Maximum	Unit
V_{oh}	Output high voltage	$I_{oh} = -4 \text{ mA}$	2.4	—	V
V_{ol}	Output low voltage	$I_{ol} = 4 \text{ mA}$	—	0.4	V
V_{ih}	Input high voltage	—	2.0	—	V
V_{il}	Input low voltage	—	—	0.8	V
I_{ip}	Input leakage current on pins with internal pull-ups (tdi and tms)	$0.0 < V_{in} < \mathbf{vdd}$	—	$+20/-1000^1$	μA
I_{oz}	Tristate output leakage current (tdo)	$0.0 < V_{out} < \mathbf{vdd}$	—	± 20	μA

¹For pins **tdi** and **tms** that have internal pull-ups, the leakage current can get to 1.0 mA when $V_{in} = 0 \text{ V}$.

3.13.2 JTAG Boundary-Scan Timing

Figure 23 shows the JTAG boundary-scan timing, and Table 38 lists the interface signal timing relationships.

Joint Test Action Group—Test Access Port

Figure 23 JTAG Boundary-Scan Timing Diagram

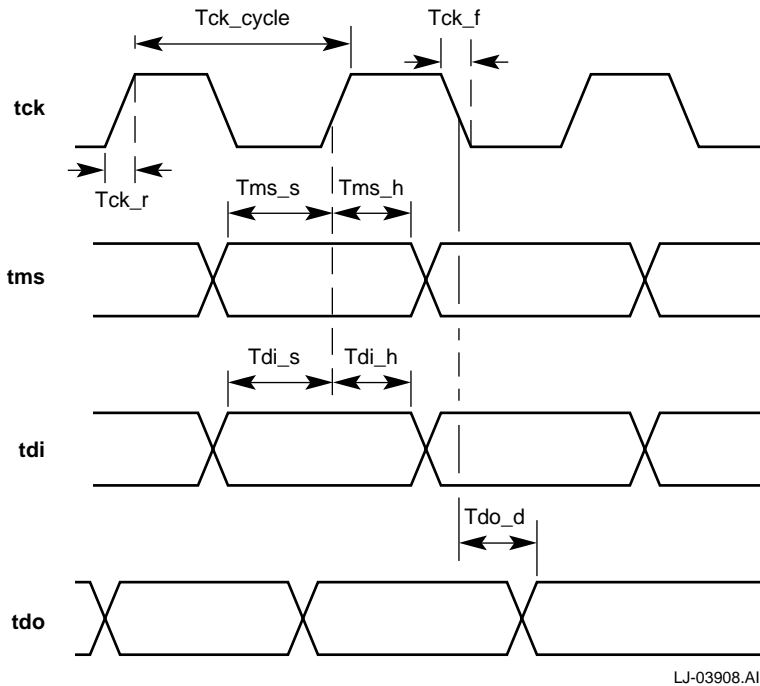


Table 38 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Unit
Tms_s	tms setup time	20	—	ns
Tms_h	tms hold time	5	—	ns
Tdi_s	tdi setup time	20	—	ns
Tdi_h	tdi hold time	5	—	ns
Tdo_d	tdo delay time	—	20	ns
Tck_r^1	tck rise time	—	3	ns
Tck_f^1	tck fall time	—	3	ns
Tck_{cycle}	tck cycle time	90	—	ns

¹Parameter design guarantee.

4 Mechanical Specifications

The 21143 is contained in either a 144-pin LQFP package type or a 144-pin MQFP package type.

Figure 24 shows the mechanical layout of the LQFP, and Table 39 lists the LQFP package dimensions in millimeters.

Figure 25 shows the mechanical layout of the MQFP, and Table 40 lists the MQFP package dimensions in millimeters.

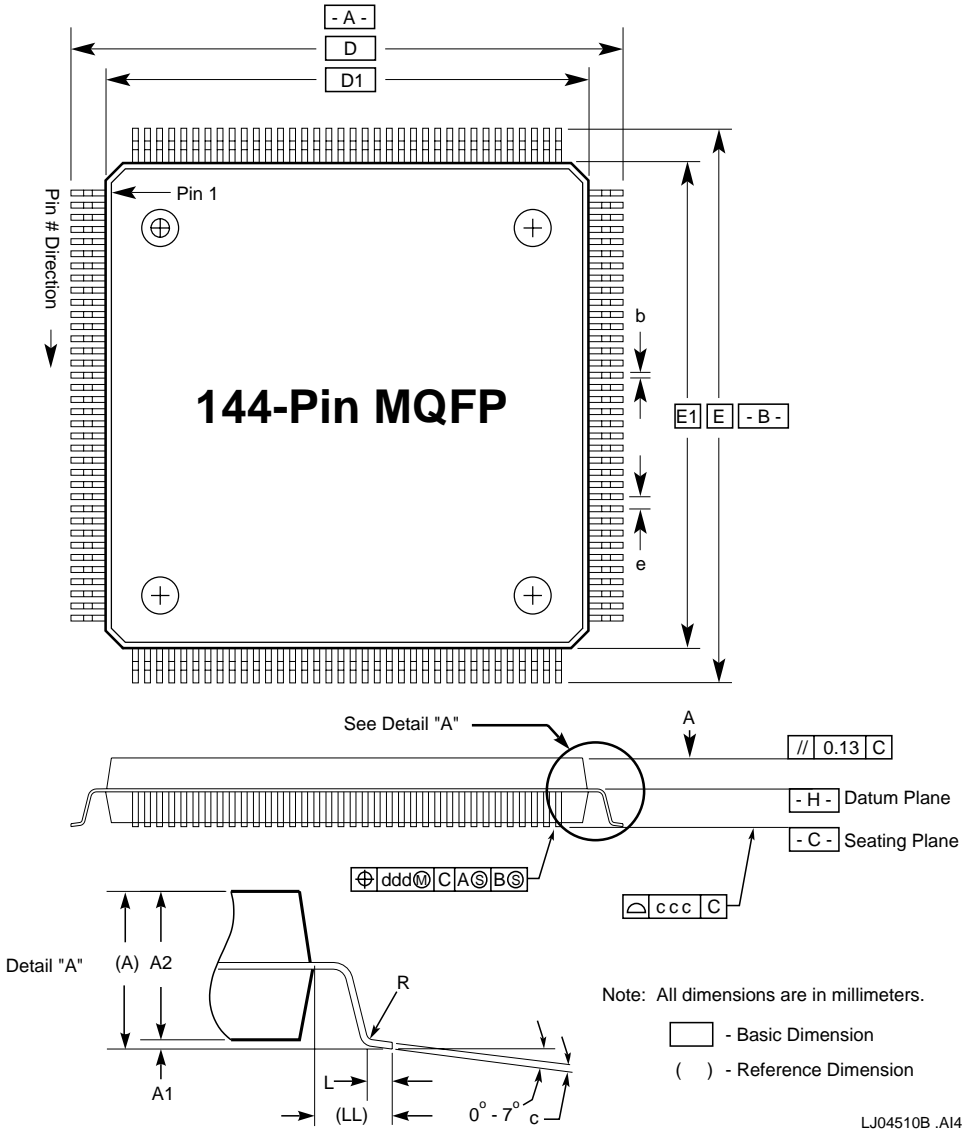
Table 39 144-Pin LQFP Package Dimensions

Symbol	Dimension	Value (mm)
LL	Lead length	1.00 reference ¹
e	Lead pitch	0.50 BSC ²
L	Foot length	0.45 minimum to 0.75 maximum
A	Package overall height	1.60 maximum
A1	Package standoff height	0.05 minimum
A2	Package thickness	1.35 minimum to 1.45 maximum
b	Lead width	0.17 minimum to 0.27 maximum
c	Lead thickness	0.09 minimum to 0.20 maximum
ccc	Coplanarity	0.08
ddd	Lead skew	0.08
D	Package overall width	22.00 BSC
D1	Package width	20.00 BSC
E	Package overall length	22.00 BSC
E1	Package length	20.00 BSC
R	Ankle radius	0.08 minimum to 0.20 maximum

¹The value for this measurement is for reference only.

²ANSI Y14.5M–1982 American National Standard Dimensioning and Tolerancing, Section 1.3.2, defines Basic Dimension (BSC) as: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. It is the basis from which permissible variations are established by tolerances on other dimensions, in notes, or in feature control frames.

Figure 25 144-Pin MQFP Package



LJ04510B .A14

Table 40 144-Pin MQFP Package Dimensions

Symbol	Dimension	Value (mm)
LL	Lead length	1.60 reference ¹
e	Lead pitch	0.65 BSC ²
L	Foot length	0.65 minimum to 1.03 maximum
A	Package overall height	4.1 maximum
A1	Package standoff height	0.25 minimum
A2	Package thickness	3.20 minimum to 3.60 maximum
b	Lead width	0.22 minimum to 0.40 maximum
c	Lead thickness	0.11 minimum to 0.23 maximum
ccc	Coplanarity	0.10
ddd	Lead skew	0.13
D	Package overall width	31.20 BSC
D1	Package width	28.00 BSC
E	Package overall length	31.20 BSC
E1	Package length	28.00 BSC
R	Ankle radius	0.13 minimum to 0.30 maximum

¹The value for this measurement is for reference only.

²ANSI Y14.5M–1982 American National Standard Dimensioning and Tolerancing, Section 1.3.2, defines Basic Dimension (BSC) as: A numerical value used to describe the theoretically exact size, profile, orientation, or location of a feature or datum target. It is the basis from which permissible variations are established by tolerances on other dimensions, in notes, or in feature control frames.

Support, Products, and Documentation

To view current product update and errata revision information, please visit the DIGITAL Semiconductor World Wide Web Internet site. You may also visit this website for technical support, a *DIGITAL Semiconductor Product Catalog*, or help deciding which documentation best meets your needs:

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Phone (U.S. and international): 1-978-568-7474
Fax: 1-978-568-6698
Electronic mail address: ctc@hlo.mts.dec.com

DIGITAL Semiconductor Products

To order the DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller and for more information about an Evaluation Board kit, contact your local distributor. The following tables list some of the semiconductor products available from DIGITAL Semiconductor.

Note: The following products and order numbers might have been revised. For the latest versions, contact your local distributor.

Chips	Order Number
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (MQFP package)	21143-PD
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller (LQFP package)	21143-TD
DIGITAL Semiconductor 21140A PCI Fast Ethernet LAN Controller	21140-AF
DIGITAL Semiconductor 21540 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller with Modem Interface (TQFP package)	21540-TA

Evaluation board kits include an evaluation board, and can include a complete design kit, an installation kit, or an accessories kit.

Evaluation Board Kits	Order Number
DIGITAL Semiconductor 21143 CardBus Evaluation Board Kit	21A43-02
DIGITAL Semiconductor 21143 PCI Evaluation Board Kit	21A43-04
DIGITAL Semiconductor 21140A 10/100BASE-TX Evaluation Board Kit	21A40-TX

DIGITAL Semiconductor Documentation

The following table lists some of the available DIGITAL Semiconductor documentation. To determine which documents apply to a particular device part number, visit the DIGITAL Semiconductor Documentation Library on DIGITAL Semiconductor's World Wide Web Internet site at:

<http://ftp.digital.com/pub/digital/info/semiconductor/literature/dsc-library.html>

Title	Order Number
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual	EC-QWC4F-TE
DIGITAL Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Product Brief	EC-QWC2B-TE
CardBus Guidelines for DIGITAL Semiconductor Ethernet Controllers: An Application Note	EC-QZ1XB-TE
DIGITAL Semiconductor 21143 Connection to the Network Using MII-based Physical Layer Devices: An Application Note	EC-QXY7A-TE
Using the DIGITAL Semiconductor 21143 with External Flash ROM, Serial ROM, and External Register: An Application Note	EC-QYZ1B-TE
Power Management in DIGITAL Semiconductor Ethernet LAN Controllers: An Application Note	EC-R96DA-TE
DIGITAL Semiconductor 21140A PCI Fast Ethernet LAN Controller Data Sheet	EC-QN7PF-TE
DIGITAL Semiconductor 21140A PCI Fast Ethernet LAN Controller Hardware Reference Manual	EC-QN7NF-TE
DIGITAL Semiconductor 21140A PCI Fast Ethernet LAN Controller Product Brief	EC-QN7MB-TE
DIGITAL Semiconductor 21540 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller with Modem Interface Product Brief	EC-R77QA-TE

Third-Party Documentation

You can order the following third-party documentation directly from the vendor.

Title	Vendor
PCI Local Bus Specification Revision 2.0	PCI Special Interest Group
PCI Local Bus Specification Revision 2.1	1-800-433-5177 (U.S.)
PCI BIOS Specification Revision 2.0	1-503-797-4207 (International)
PCI BIOS Specification Revision 2.1	1-503-234-6762 (FAX)
Institute of Electrical and Electronics Engineers (IEEE) 802.3 and 1149.1	IEEE Service Center 1-800-701-4333 (U.S.) 1-908-981-0060 (International) 1-908-981-9667 (FAX)